AMENDMENTS TO THE CLAIMS:

Please cancel claim 2, without prejudice. Kindly amend claims 1, 3, 5, 6, 8 and 9, and add new claims 10-12, as shown below.

This listing of claims will replace all prior versions and listings of claims in the Application:

Claim 1 (currently amended): An image rejection mixer which comprises:

~~distribution means~~ a signal distributor supplied with local signals having a phase difference in order to distribute said local signals;

a first and a second ~~mixing means~~ signal mixer for mixing the distributed local signals and RF signals having phases different from those of said distributed local signals and for outputting respective IF current signals;

a first and a second phase ~~shift means~~ shifter for generating a 90 degree phase difference between said respective IF current signals; and

~~addition means~~ a signal adder for adding the phase shifted respective IF current signals,

wherein image signals are removed from said respective RF signals, and

wherein said first and said second phase shifters comprise a lattice circuit having inductors and resistors.

Claim 2 (canceled)

Claim 3 (currently amended): The image rejection mixer according to claim 1, wherein said ~~addition means~~ signal adder comprises a feedback loop, and adds said IF current signals.

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Claim 4 (original): The image rejection mixer according to claim 1, wherein said feedback loop is a feedback loop of positive feedback.

Claim 5 (currently amended): The image rejection mixer according to claim 1, wherein said ~~addition means~~ signal adder comprises a differential amplifier.

Claim 6 (currently amended): The image rejection mixer according to claim 1, which further comprises:

a first impedance between said first ~~mixing means~~ signal mixer and said first phase ~~shift means~~ shifter; and

a second impedance between said second ~~mixing means~~ signal mixer and said second phase ~~shift means~~ shifter.

Claim 7 (original): The image rejection mixer according to claim 6, wherein said impedances comprises a resistor, a capacitor, or an inductor or an arbitrary combination of them.

Claim 8 (currently amended): The image rejection mixer according to claim 7, wherein values of said impedances are determined on the basis of a phase difference between said IF current signal outputted from said first ~~mixing means~~ signal mixer and said IF current signal outputted from said second ~~mixing means~~ signal mixer.

Claim 9 (currently amended): A receiver including an image rejection mixer which comprises:

~~receiving means~~ a signal receiver for receiving RF frequency signals having a phase difference; and

an image rejection mixer including:

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~~distribution means~~ a signal distributor supplied with local signals having a phase difference in order to distribute said local signals;

a first and a second ~~mixing means~~ signal mixer for mixing the distributed local signals and said RF signals having phases different from those of said distributed local signals and for outputting respective IF current signals;

a first and a second phase ~~shift means~~ shifter for generating a 90 degree phase difference between said respective IF current signals; and

~~addition means~~ a signal adder for adding the phase shifted respective IF current signals,

wherein image signals are removed by said image rejection mixer from said respective RF signals received by said ~~receiving means~~ signal receiver.

Claim 10 (new): An image rejection mixer, comprising:

a signal distributor which outputs LO signals having a phase difference;

a first and a second gilbert cell mixer including:

a current source;

a pair of transistors, each transistor having a collector, base and emitter in which each emitter is connected to said current source through a resistor; and

two pairs of transistors having collectors, bases and emitters, in which two coupled emitters of each pair of said two pairs of transistors are connected to each collector of said pair of transistors, one of the collectors of one transistor in one pair of said two pairs of transistors is connected to one of the collectors of one transistor in the other pair of said two pairs of transistors, balanced RF signals are input into each base of each transistor of said pair of transistors, phase differenced balanced LO signals are input to the base of each transistor of

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each of said two pairs of transistors, and balanced IF current signals are output from each collector of each transistor of said two pairs of transistors;

a first and a second phase shifter including an LR lattice circuit in which said balanced IF current signals are input and phase shifted balanced IF current signals are output; and

a signal adder including two pairs of cascode transistors having collectors, bases and emitters in which each collector of one pair of cascode transistors is connected to the collectors of another pair of cascode transistors, and each of the emitters in each transistor of each pair of cascode transistors is connected to said first and second phase shifter.

Claim 11 (new): An image rejection mixer, comprising:

a signal distributor for outputting LO signals having a phase difference;

a first and a second gilbert cell mixer including:

a current source;

a pair of transistors, each transistor having a collector, base and emitter in which each emitter is connected to said current source through a resistor; and

two pairs of transistors having collectors, bases and emitters, in which two coupled emitters of each pair of said two pairs of transistors are connected to each collector of said pair of transistors, one of the collectors of one transistor in one pair of said two pairs of transistors is connected to one of the collectors of one transistor in the other pair of said two pairs of transistors, balanced RF signals are input into each base of each transistor of said pair of transistors, phase differenced balanced LO signals are input to the base of each transistor of each of said two pairs of transistors, and balanced IF current signals are output from each collector of each transistor of said two pairs of transistors;

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a first and a second phase shifter including a LR lattice circuit in which said balanced IF current signals are input and phase shifted balanced IF current signals are output; and

a signal adder including:

cascode transistors having collectors, bases and emitters;

a differential amplifier comprising:

a current source; and

a differential pair of transistors having collectors, bases and emitters, said emitters being coupled, and each base of each transistor of said differential pair of transistors is connected to said first and said second phase shifters, said coupled emitters of said differential pair of transistors are connected to said current source, and each collector of each transistor of said differential pair of transistors is connected to the bases of said cascode transistors; and

resistors located between the collectors of the differential pair of transistors and a voltage source.

Claim 12 (new): A receiver including an image rejection mixer which comprises:

a signal receiver for receiving RF frequency signals having a phase difference; and

an image rejection mixer including:

a signal distributor supplied with local signals having a phase difference in order to distribute said local signals;

a first and a second signal mixer for mixing the distributed local signals and said RF signals having phases different from those of said distributed local signals and for outputting respective IF current signals;

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a first and a second phase shifter for generating a 90 degree phase difference between said respective IF current signals; and

a signal adder for adding the phase shifted respective IF current signals,

wherein image signals are removed by said image rejection mixer from said respective RF signals received by said signal receiver, and

wherein said first and said second phase shifters comprise a lattice circuit having inductors and resistors.

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